

## CLAIMS

What is claimed is:

- 1           1. A method for designing a system on a target device utilizing field programmable gate  
2 arrays (FPGAs), comprising:  
3           placing new logic elements (LEs) at preferred locations on a layout of an existing system;  
4 and  
5           resolving illegalities in placement of the new LEs.
- 1           2. The method of Claim 1, wherein resolving illegalities in the placement of the new LEs  
2 comprises:  
3           generating proposed moves for an LE;  
4           generating cost function values for a current placement and placements with the proposed  
5 moves; and  
6           accepting a proposed move if its associated cost function value is better than the cost  
7 function value for the current placement.
- 1           3. The method of Claim 1, wherein resolving illegalities in the placement of the new LEs  
2 comprises:  
3           generating a proposed move for an LE;  
4           generating cost function values for a current placement and a placement with the  
5 proposed move; and  
6           accepting the proposed move if its associated cost function value is better than the cost  
7 function value of the current placement.
- 1           4. The method of Claim 2, wherein generating the proposed moves comprises moving  
2 the LE to a logic-array block (LAB) that is a fanin of the LE.

1           5. The method of Claim 2, wherein generating the proposed moves comprises moving  
2 the LE to a logic-array block (LAB) that is a fanout of the LE.

1           6. The method of Claim 2, wherein generating the proposed moves comprises moving  
2 the LE to a logic-array block (LAB) that is a sibling of a LAB where the LE resides.

1           7. The method of Claim 2, wherein generating the proposed moves comprises moving  
2 the LE to a logic-array block (LAB) that is adjacent to the LE.

1           8. The method of Claim 2, wherein generating the proposed moves comprises moving  
2 the LE to any random free LE.

1           9. The method of Claim 2, wherein generating the proposed moves comprises moving  
2 the LE in a direction of a critical vector.

1           10. The method of Claim 2, wherein generating the cost function values comprises  
2 computing values using cluster legality as a parameter.

1           11. The method of Claim 10, wherein the cluster legality is a function of a number of  
2 legal LEs in a LAB.

1           12. The method of Claim 10, wherein the cluster legality is a function of a number of  
2 legal inputs in a LAB.

1           13. The method of Claim 10, wherein the cluster legality is a function of a number of  
2 legal outputs in a LAB.

1           14. The method of Claim 2, wherein generating the cost function values comprises  
2 computing values using timing cost as a parameter.

1           15. The method of Claim 2, wherein generating the cost function values comprises  
2 computing values using wire length cost as a parameter.

1           16. The method of Claim 2, further comprising modifying a cost function.

1           17. The method of Claim 16, wherein modifying the cost function comprises increasing a  
2 penalty on a reoccurring illegality.

1           18. A method for designing a system on field programmable gate array (FPGAs),  
2 comprising:  
3           determining placement of logic elements (LEs) for an existing system;  
4           modifying a design for the existing system to improve performance;  
5           placing new LEs from a modified design on the placement of LEs for the existing system;  
6           and  
7           resolving illegalities in placement of the new LEs.

1           19. The method of Claim 18, wherein modifying the design for the existing system to  
2 improve performance comprises:  
3           estimating routing delays for the existing system; and  
4           adding LEs to the existing system to reduce the routing delays.

1           20. The method of Claim 18, wherein resolving the illegalities in the placement of the  
2 new LEs comprises:  
3           generating proposed moves for an LE;  
4           generating cost function values for a current placement and placements with the proposed  
5 moves; and  
6           accepting a proposed move if its associated cost function value is better than a cost  
7 function value for the current placement.

1           21. The method of Claim 20, wherein generating the cost function values comprises  
2 computing values using cluster legality as a parameter.

1           22. The method of Claim 20, wherein generating the cost function values comprises  
2 computing values using timing cost as a parameter.

1           23. The method of Claim 20, wherein generating the cost function values comprises  
2 computing values using wire length cost as a parameter.

1           24. The method of Claim 20, further comprising modifying a cost function.

1           25. The method of Claim 24, wherein modifying the cost function comprises increasing a  
2 penalty on a reoccurring illegality.

1           26. A machine-readable medium having stored thereon sequences of instructions, the  
2 sequences of instructions including instructions which, when executed by a processor, causes the  
3 processor to perform:

4 placing new logic elements (LEs) at preferred locations on a layout of an existing system;  
5 and  
6 resolving illegalities in placement of the new LEs.

1 27. The machine-readable medium of Claim 26, wherein resolving illegalities in the  
2 placement of the new LEs comprises:  
3 generating proposed moves for an LE;  
4 generating cost function values for a current placement and placements with the proposed  
5 moves; and  
6 accepting a proposed move if its associated cost function value is better than the cost  
7 function value for the current placement.

1 28. The machine-readable medium of Claim 27, wherein generating the cost function  
2 values comprises computing values using cluster legality as a parameter.

1 29. The machine-readable medium of Claim 26, further comprising instructions, which  
2 when executed, causes the processor to further perform modifying a cost function by increasing a  
3 penalty on a reoccurring illegality.